Applicants' Claim 1 includes the following:

> "a pipeline execution circuit to process a first predetermined number of instructions simultaneously, each of said first predetermined number of instructions being in a respectively different stage of execution within said pipeline execution circuit, instructions being capable of advancing to a next stage of execution within said pipeline execution circuit at a time determined by the system clock signal; and
>
> a pipeline fetch circuit coupled to provide each of the first predetermined number of instructions directly to said pipeline execution circuit, the pipeline fetch circuit to retain a second predetermined number of instructions simultaneously, each of said second predetermined number of instructions being in a respectively different stage of processing within said pipeline fetch circuit, an instruction being capable of advancing to a next stage of execution within said pipeline fetch circuit at a time determined by the system clock signal and independently of the times at which instructions advance to a next stage of execution within said pipeline execution circuit."

As best understood, the Examiner is stating that Bhamidipati teaches Applicants' Claim 1 as follows:

The Examiner states that Applicants' fetch circuit is taught by elements 300, 302, 304, and 308 of Bhamidipati Figure 3 (Office Action page 3, last line). Thus, Applicants' fetch circuit is being equated with the fetch (F) and decode (D) stages of the Bhamidipati pipeline. (See Bhamidipati Figures 1 and 3.) Bhamidipati stages A and X must therefore comprise Applicants' pipeline execution circuit. If this understanding of the Examiner's rejection is incorrect and the current rejection is not withdrawn, clarification is respectfully requested.

According to the foregoing, Bhamidipati teaches a pipeline that decouples stages F and D of the fetch circuit by inserting a decoupling queue, as shown in Bhamidipati Figure 3. Despite the fact that stages F and D are decoupled, instructions move from stage D of the fetch circuit to stage A of the execution circuit *in lock step*. That is, after an instruction is retrieved from the decoupling queue, the instruction moves from fetch stage D to execution stage A in a manner that requires that if stage A stalls, stage D will also stall, and if stage D stalls, stage A will empty. Thus, Bhamidipati does not teach or

suggest Applicants' system of Claim 1 that allows an instruction to advance within a next stage of a fetch circuit at a time the is independent of the way in which instructions advance within an execution circuit coupled to the fetch circuit.

Next, it may be noted that Bhamidipati states that the decoupling queue may be inserted between other pipe stages. (Bhamidipati column 3 lines 53-57.) Consider, therefore, a system that inserts the decoupling queue between stages D and A of the Bhamidipati pipeline. That is, the decoupling queue links what is being referred to in this discussion as the Bhamidipati fetch and execution circuits. In this embodiment, the Bhamidipati fetch circuit is not coupled to provide instructions directly to the execution circuit as is claimed by Applicants' Claim 1. Instead, the Bhamidipati instructions are provided from the fetch circuit to the queue, and are then retrieved by the execution circuit. This results in a delay between the time an instruction completes decode in stage D and the start of operand address computation. While it is true that the Bhamidipati overlapping read and write signals help to minimize this delay, this delay cannot be entirely eliminated. Thus Applicants' system of Claim 1 provides superior throughput, since even though the fetch and execution circuits allow instructions to independently advance, the fetch circuit is coupled to provide instructions directly to the execution circuit.

Next, the Examiner's comments regarding the combination of Bhamidipati and Hayes are considered. First, the Examiner states that although Bhamidipati did not disclose a fetch circuit that transfers an instruction directly to an execution stage, Hayes does teach this aspect of Applicants' invention. This statement is not understood based on the fact that the Examiner cited Bhamidipati stages F and D as teaching Applicants' fetch circuit. (Office Action page 3 last line, citing elements 300, 302, 304, and 308 of Bhamidipati Figure 3 as teaching Applicants' fetch circuit.) If the Examiner's analysis is followed, it would appear that the Bhamidipati fetch stage D provides an instruction directly to execution stage A. Thus, the citing of Hayes as teaching this aspect of a pipeline system appears unnecessary.

Despite the fact that the teaching of Hayes seems superfluous in regards to Claim 1, Hayes will never-the-less be discussed. Although Hayes may disclose fetch

and execution stages that are directly coupled as stated by the Examiner, it is important to note that Applicants' Claim 1 is claiming a fetch circuit that is directly coupled to an execution circuit in a way that *allows instructions to advance within* stages of the *fetch circuit independently* of the advancement of instructions within stages of the *execution circuit*. This is not taught by Bhamidipati or Hayes, alone or in combination.

As already discussed above with respect to the Bhamidipati system, Bhamidipati does not teach the foregoing aspects Applicants' Claim 1 regardless of whether the decoupling queue is inserted between the F and D stages, the D and A stages, or any other stages, of the pipeline. Similarly, Hayes does not teach the aspects of Applicants' Claim 1 where the fetch and execution circuits are directly coupled *yet independently operable*. In particular, in the Hayes system, instructions advance in lock step between all stages of the pipeline, including between the fetch and execution stages. Hayes provides no teaching or suggestion whatsoever on allowing instructions to advance within fetch stages independently of instruction advancement within the execution stages.

Moreover, it should be noted that Hayes discusses the problems caused by the variability of fetch and execution times for instructions included within a complex instruction set. However, the only solution offered by Hayes involves allowing some instructions to by-pass some of the pipeline stages. (Hayes page 224, last paragraph.) Thus, although Hayes recognizes some of the problems solved by Applicants' invention, Hayes actually *teaches away* from Applicants' invention by suggesting that instructions should *by-pass* pipeline stages rather than being passed *directly between* those stages, as Applicants' invention allows.

For at least the foregoing reasons, Hayes does not add anything to Bhamidipati that teaches or suggests Applicants' invention.

Next, the Examiner states that it would have been obvious to implement Bhamidipati's pipeline as a fetch stage directly coupled to an execution stage as found in Hayes' teaching. (Office Action page 5, lines 1-4.) Although this statement is not completely understood, it will be assumed that the Examiner is stating that the entire circuit disclosed in Bhamidipati is to be considered the fetch circuit, and the Hayes

execution stage is to be added directly to this fetch circuit. Thus, the Bhamidipati stages F, D, A and X are analogous to Applicants' fetch circuit, and the Hayes execution stage is analogous to Applicants' execution circuit. If this understanding of the Examiner's discussion is incorrect and this rejection is maintained, clarification is requested.

In regards to the foregoing configuration, instructions retrieved from the decoupling queue of Bhamidipati will advance *in lock step* between the Bhamidipati stages D, A, and X to the Hayes execution stage. A stall in any one of these stages will stall all preceding ones of these stages and empty the subsequent stages. While it is true that the decoupling queue will decouple fetch stage F from the rest of the fetch stages D, A, and X and the Hayes execution stages, instructions *will not advance independently* within fetch stages as compared to the way the instructions advance within the execution stage. Once again, it should be noted that nothing in Bhamidipati or Hayes describes how to achieve this type of independent operation between a fetch and execution circuit that are directly coupled. For this additional reason, this rejection is improper and should be withdrawn.

Furthermore, it is submitted that one skilled in the art would not be motivated to make the cited combination for several reasons. Hayes, which was published in 1978, discloses a simple pipeline design of the type discussed in the Bhamidipati background section. Bhamidipati discusses prior art improvements to this type of pipeline, including the addition of a decoupling queue. (Bhamidipati column 1 lines 12-25.) Bhamidipati then discloses the further improvement involving the use of non-overlapping read and write signals to access this decoupling queue. Therefore, Bhamidipati itself discusses the type of prior art system disclosed in Hayes, including the problems associated therewith, and suggests improvements to address these drawbacks. In light of this teaching in Bhamidipati , one skilled in the art would not be motivated to combine the teaching of Hayes and Bhamidipati.

Moreover, the Examiner's assertion that one skilled in the art would be motivated to utilize the Bhamidipati pipeline as a fetch circuit to which the Hayes execution stage is directly coupled is not understood. Bhamidipati teaches a complete pipeline that

includes all necessary fetch and execution stages. There is no need to add any other execution stages, much less an execution stage as taught by Hayes. Additionally, there appears to be absolutely no motivation to convert the entire Bhamidipati pipeline into a fetch circuit coupled to an additional execution stage, much less any direction on how this might be accomplished. Thus, it appears the Examiner is merely attempting to piece together Applicants' invention in hindsight, a practice that has long been held impermissible.

Finally, as discussed above, although Hayes appears to recognize the problems associated with variable instruction fetch and execution times, the Hayes solution to these problems involves allowing instructions to bypass pipeline stages. This teaches away from Applicants' solution of passing instructions directly between various stages while at the same time allowing instructions to advance independently within fetch stages as compared to execution stages.

For all of the foregoing reasons, nothing in Bhamidipati or Hayes, alone or in combination, teaches Applicants' invention of Claim 1. It is respectfully submitted that this rejection is improper, and should be withdrawn.

Next, independent Claims 21, 27, 32, 40 and 46 are considered. Each of these Claims include aspects of Applicants' invention that are similar to those discussed above with respect to Claim 1. For similar reasons, these Claims are also allowable over the current rejection, which is improper, and should be withdrawn.

Finally, dependent Claim 39 is considered. This Claim depends from Claim 32 and is allowable for at least the reasons discussed above in reference to Claims 1 and 32.

To summarize, Claims 1, 21, 27, 32, 39, 40 and 46 are not taught or suggested by the cited combination of references, and are allowable over this rejection, which should be withdrawn.

3. Claims 2-6, 22-25, 28-30, 33-38, 41-43, and 45 were rejected under 35 USC 103(a) as being unpatentable over Bhamidipati in view of Hayes, and further in view of

U.S. Pat. No. 6, 026, 477 to Kyker et al. (hereinafter "Kyker"). This rejection is respectfully traversed.

Claims 2-6 depend directly or indirectly from Claim 1 and are allowable over the current rejection for reasons similar to those discussed above in reference to Claim 1. These Claims include additional aspects not taught or suggested by the cited combination of references as follows.

Claim 3 includes the aspect of a pre-decode stage in the pipeline fetch circuit, wherein an instruction can enter this stage independently of the way in which instructions are advancing through the stages of the execution circuit. The Examiner states this aspect is taught by Kyker, which describes the use of multiple decode stages. While it may be true that Kyker discloses multiple decode stages, Kyker in no way teaches entry of an instruction into a pre-decode stage independently of the movement of instructions through an execution circuit. Moreover, none of the other references teach this type of functionality. For this additional reason. For example Claim 3 is allowable over this rejection.

Claim 4 depends from Claim 3, and is allowable for the reasons discussed above in reference to Claim 3. Additionally, Claim 4 includes entry of an instruction into a decode stage of a pipeline from the pre-decode stage independently of movement of instructions through the execution circuit. The Examiner states this is taught by the disclosure of multiple decode stages in Kyker. Again, this mention of multiple decode stages does not teach the movement of an instruction from a pre-decode stage into a decode stage independently of the movement of instructions through the execution circuit. Moreover, none of the other references teach this aspect of Applicants' invention. For this additional reason, Claim 4 is allowable over this rejection.

Claims 5 and 6 depend directly or indirectly from Claim 4, and are allowable for at least the reasons discussed above in reference to Claim 4.

Claims 22-25 depend directly or indirectly from Claim 21 and are allowable over the current rejection for at least the reasons discussed above in reference to Claim 21. These Claims further describe additional aspects not taught by the cited combination of

references. For example, Claim 25 describes the aspect of Applicants' invention wherein an instruction may be retrieved from a queue for presentation to at least one of the fetch stages regardless of whether instructions are advancing with the execution stages. This is not taught by any of the references.

In reference to Claim 25, the Examiner states that the Bhamidipati decoupling queue "...allows the circuit to remain independent of the execution stages". (Office Action page 18, last full paragraph.) Applicants' Representative does not agree. When inserted between fetch stages F and D as shown in Figure 3, the queue decouples the fetch stages. However, an instruction cannot enter fetch stage D without the instructions advancing within both of execution stages A and X. Thus, an instruction cannot be retrieved from the queue for presentation to a Bhamidipati fetch stage independently of whether instructions are advancing within the execution stages. Furthermore, if the Bhamidipati decoupling queue were instead inserted between fetch stage D and execution stage A, an instruction would not be fetched from the queue for presentation to a fetch stage at all, since the instruction would be presented instead to execution stage A. Thus, Bhamidipati does not teach or suggest this aspect of Applicants' invention, and Claim 25 is allowable over this rejection for this additional reason.

Claims 28-30 depend directly or indirectly from Claim 27 and are allowable over the current rejection for at least the reasons discussed above in reference to Claim 27.

Claims 33-38 depend directly or indirectly from Claim 32 and are allowable over the current rejection for at least the reasons discussed above in reference to Claim 32. These Claims include additional aspects not taught or suggested by the cited combination of references.

For example, Claim 35 describes a queue that is coupled to provide an instruction to the fetch circuit irrespective of whether an instruction is provided from the fetch circuit to the execution circuit. For reasons similar to those discussed above in reference to Claim 25, this aspect of Applicants' invention is not taught or suggested by

the cited combination of references, and this Claim is therefore allowable over the current rejection.

Claims 36 and 37 depend from Claim 35, are allowable for at least the reasons discussed above in reference to Claim 35.

Claim 38 depends from Claim 37, and is allowable for at least the reasons discussed above in reference to Claim 35. This Claim further describes the aspect wherein one of the fetch stages includes a circuit to allow retrieval of an instruction from either a memory or from a queue. As discussed above, this aspect is clearly shown in Applicants' Figure 10 and is further discussed in the Specification. The Examiner states this aspect is taught by Kyker, since Kyker demonstrates a fetch queue that temporarily stores instructions that were retrieved from memory in preparation for entry into a fetch stage of a pipeline. While Kyker may disclose a fetch queue, Kyker does not teach or suggest allowing for retrieval of an instruction from either the memory or from the queue. For this additional reason, Claim 38 is allowable over this rejection.

Claims 41-43 and 45 depend from Claim 40 and are allowable over this rejection for at least the reasons discussed above in reference to Claim 40.

To summarize, Claims 2-6, 22-25, 28-30, 33-38, 41-43, and 45 are not taught or suggested by the cited combination of references, and are allowable over this rejection, which should be withdrawn.

4. Claim 7 was rejected under 35 USC 103(a) as being unpatentable over Bhamidipati in view of Hayes and Kyker, and further in view of U.S. Patent No. 5,577,259 to Alferness et al. (hereinafter "Alferness"). This rejection is respectfully traversed.

Claim 7 depends from Claim 5 and is allowable for at least the reasons discussed above in reference to Claim 5. In addition, Claim 7 describes the aspect wherein the pipeline includes a microcode-controlled sequencer to control execution of extended stages of extended-mode instructions. The system includes a control circuit to allow an instruction to enter a pre-decode stage of processing while extended-mode instructions are not advancing within the execution circuit. The Examiner states these

aspects are taught by the cited combination of references. Applicants' Representative disagrees. None of the references teaches or suggests, alone or in combination, a system for allowing an instruction to enter a pre-decode stage of a pipeline while extended-mode instructions are not advancing within an execution circuit. It appears the invention is being impermissibly pieced together in hindsight. It is respectfully submitted that Claim 7 is not taught or suggested by the cited combination of references, and is allowable over this rejection.

5. Claims 26, 31, and 44 were rejected under 35 USC 103(a) as being unpatentable over Bhamidipati in view of Hayes and further in view of Alferness. This rejection is respectfully traversed.

Claim 26 depends from Claim 21 and is allowable over this rejection for at least the reasons discussed above in reference to Claim 21.

Claim 31 depends from Claim 27 and is allowable over this rejection for at least the reasons discussed above in reference to Claim 27.

Claim 44 depends from Claim 40 and is allowable over this rejection for at least the reasons discussed above in reference to Claim 40.

In sum, Claims 26, 31, and 44 are not taught or suggested by the cited combination of references, and this rejection should be withdrawn.

6. The Examiner objects to the Amendment filed April 30, 2003 based on the assertion that new matter was introduced into the disclosure. As discussed above in Section 1, it is respectfully submitted that all Claims presented by that amendment are fully supported by the Specification and the Drawings. If this objection is not withdrawn, more clarification is requested as to the material that is believed to be unsupported.

Conclusion

In the Office Action dated June 19, 2003, Claims 1-7 and 21-46 were rejected. These Claims remain as previously presented. In view of the arguments set forth above, it is submitted that the Claims are allowable over the current rejection and an early Notice of Allowance is respectfully requested. If the Examiner has any questions or concerns, a call to the undersigned is welcomed and encouraged.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited in the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, P O Box 1450, Alexandria, VA 22313-1450 on October 20, 2003.

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Signature

October 20, 2003